What we claim is:

1. A parallel signal transmission device comprising:

a transmitting unit, for converting serial signals into parallel signals to be transmitted, provided with a latch for periodically latching the parallel signals besides the transmitted parallel signals, a code signal generator for generating serial code signals including synchronizing signals from the signals latched at the latch, and a fixed delay portion for adjusting phases of the parallel signals to the serial code signals by delaying the parallel signals by a predetermined delay time; and

a receiving unit, for receiving the parallel signals, provided with a clock recovery portion of the parallel signals and the serial code signals, a bit changeover portion for changing over bits of the parallel signals and the serial code signals based on clocks recovered by the clock recovery portion, a bit shift detector for detecting bit shift amounts of the parallel signals outputted from the bit changeover portion based on the serial code signals, and a variable delay portion for performing skew adjustments of the parallel signals outputted from the bit changeover portion depending on the bit shift amounts.

2. The parallel signal transmission device as claimed in claim 1 wherein the transmitting unit is further provided with a scrambler for scrambling the parallel signals to be furnished to the latch and the fixed delay portion, and the receiving unit is further provided with a descrambler for descrambling the parallel signals outputted from the variable delay portion.

3. The parallel signal transmission device as claimed in claim 2 wherein the latch resets the scrambler at a timing the latch latches the parallel signals, and the bit shift detector resets the descrambler at a timing the bit shift detector performs skew adjustments to the variable delay portion.

4. The parallel signal transmission device as claimed in any one of

claims 1 to 3 wherein a parallel number in the parallel signals comprises a prime number.

5. The parallel signal transmission device as claimed in any one of claims 1 to 4 wherein a parallel number in the parallel signals and a bit number at a sampling interval latched by the latch are mutually in a prime relationship.

6. The parallel signal transmission device as claimed in any one of claims 1 to 5 wherein the bit shift detector has a detecting unit for detecting the bit shift amounts of the parallel signals from the synchronizing signals by performing a code matching between the serial code signals paralleled and parallel signals outputted from the bit changeover portion.

7. The parallel signal transmission device as claimed in claimed 6 wherein the bit shift detector has a code matching unit for performing the code matching using windows of a predetermined bit number based on the synchronizing signals, and the predetermined delay time of the fixed delay portion comprises a phase adjustment time for the windows.

8. The parallel signal transmission device as claimed in any one of claims 1 to 7 wherein the bit shift detector detects the bit shift amounts of the parallel signals in a predetermined stage of forward and backward protection units.

9. The parallel signal transmission device as claimed in claim 8 wherein the bit shift detector has a determining unit for determining a synchronization established state where the bit shift amounts are detected only when a protection is established by only one of the protection units.

10. The parallel signal transmission device as claimed in claim 9 wherein the bit shift detector has a prohibiting unit for prohibiting the code matching at timings other than timings of synchronizing signals when the synchronization established state is obtained.

11. The parallel signal transmission device as claimed in claim 9 or 10 wherein the bit shift detector has a clearing unit for clearing the protection units of the corresponding parallel signals when the synchronization established state is not obtained.

12. The parallel signal transmission device as claimed in any one of claims 1 to 11 wherein the bit shift detector has a warning unit for generating a warning when the synchronization established state is not obtained for a predetermined time.